WHAT IS CLAIMED IS:

1. An EEPROM integrated circuit structure, the structure comprising: a substrate including a surface region, the surface region being provided within a first cell region; a gate dielectric layer of first thickness overlying the surface of the substrate region; a select gate overlying a first portion of the gate dielectric layer; a floating gate floating gate overlying a second portion of the gate dielectric layer and coupled to the select gate;

an insulating layer overlying the floating gate; a control gate overlying the floating gate overlying the insulating layer and coupled to the floating gate; a tunnel window provided in a stripe configuration within a portion of the gate dielectric layer, the portion of the gate dielectric layer being of a second thickness, the second thickness being less than the first thickness.

2. The structure of claim 1 wherein the gate dielectric layer comprises a silicon dioxide.

3. The structure of claim 1 wherein the tunnel window is characterized by a width of less than 0.25 microns.

4. The structure of claim 1 wherein the insulating layer is an ONO layer coupled between the floating gate and the control gate.

5. The structure of claim 1 wherein the floating gate has a design width of 1.5 microns.

6. The structure of claim 1 wherein the tunnel window is provided using a phase shift mask.

7. The structure of claim 1 wherein the stripe configuration extends through a plurality of cells, each of the cells being separated by a field oxide region.

8. The structure of claim 1 wherein the substrate is a semiconductor wafer.

9. The structure of claim 1 wherein the select gate, floating gate, and control gate are provided within a cell region, the cell region being provided within an isolation region.

10. The structure of claim 1 wherein the stripe configuration runs through the first cell region to other cell regions numbered from 2 through N, where N is an integer greater than 2.

11. An EEPROM integrated circuit structure, the structure comprising: providing a substrate including a surface region, the surface region being provided within a first cell region; forming a gate dielectric layer of first thickness overlying the surface of the substrate region; patterning the gate dielectric layer to form a plurality of stripes, each of the stripes being characterized by a second thickness, the second thickness being less than the first thickness, each of the stripes having a predetermined width and a predetermined length, at least one of the stripes including a stripe portion traversing through a portion of the first cell region and other cell regions;

forming a floating gate overlying a portion of the gate dielectric layer, the portion of the gate dielectric layer including the strip portion traversing through the portion of the gate dielectric layer;

forming an insulating layer overlying the floating gate; forming a control gate overlying the floating gate overlying the insulating layer and coupled to the floating gate; and

wherein the stripe portion traverses through the portion of the first cell region includes a tunnel window for a memory device.

12. The method of claim 11 wherein the gate dielectric Idyer comprises a silicon dioxide.

13. The method of claim 11 wherein the tunnel window is characterized by a width of less than 0.25 microns.

14. The method of claim 11 wherein the insulating layer is an ONO layer coupled between the floating gate and the control gate.

15. The method of claim 11 wherein the floating gate has a design width of 1.5 microns.

16. The method of claim 11 wherein the tunnel window is provided using a phase shift mask.

17. The method of claim 11 wherein the stripe configuration extends through a plurality of cells, each of the cells being separated by a field oxide region.

18. The method of claim 11 wherein the substrate is a semiconductor wafer.

19. The method of claim 11 wherein the floating gate and the control gate are provided within a cell region, the cell region being provided within an isolation region.

20. The method of claim 11 wherein the stripe configuration runs through the first cell region to the other cell regions, the other cell regions being numbered from 2 through N, where N is an integer greater than 2.